



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Kinter *et al.*

Appl. No.: 09/836,541

Filed: April 18, 2001

For: **Mapping System and Method for  
Instruction Set Processing**

Confirmation No.: 6813

Art Unit: 2183

Examiner: Pan, Daniel H.

Atty. Docket: 1778.0200000 (0128.00US)

**Supplemental Information Disclosure Statement**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

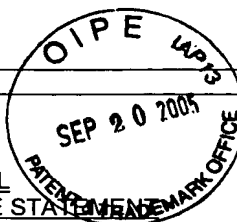
Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98. The numbering on this Supplemental Information Disclosure Statement is a continuation of the numbering in Applicants' initial Information Disclosure Statement filed September 28, 2004, in the above-captioned application.

Applicants have listed publication dates on the accompanying Form PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

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180.00 DP



FORM PTO-1449

SUPPLEMENTAL  
INFORMATION DISCLOSURE STATEMENTATTY. DOCKET NO.  
1778.0200000APPLICATION NO.  
09/836,541FIRST NAMED INVENTOR  
Ryan C. KinterFILING DATE  
April 18, 2001ART UNIT  
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## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA1	3,631,405	12/1971	Hoff <i>et al.</i>			
	AB1	3,794,980	02/1974	Cogar <i>et al.</i>			
	AC1	3,811,114	05/1974	Lemay <i>et al.</i>			
	AD1	3,840,861	10/1974	Amdahl <i>et al.</i>			
	AE1	3,983,541	09/1976	Faber <i>et al.</i>			
	AF1	4,110,822	08/1978	Porter <i>et al.</i>			
	AG1	4,149,244	04/1979	Anderson <i>et al.</i>			
	AH1	4,229,790	10/1980	Gilliland <i>et al.</i>			
	AI1	4,295,193	10/1981	Pomerene, James H.			
	AJ1	4,432,056	02/1984	Aimura, Harutsugu			

## FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AK1	EP 0 073 424 A2	03/1983	Europe			N/A

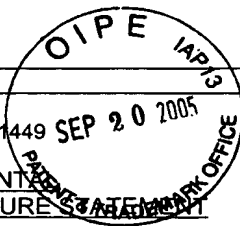
## OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AO1	U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (9 pages).
	AP1	Preliminary Amendment, filed February 1, 2002, in U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (15 pages).
	AQ1	Case, Brian, "ARM Architecture Offers High Code Density: Non-Traditional RISC Encodes Many Options in Each Instruction," <i>Microprocessor Report</i> , Vol. 5, No. 23, pgs. 11-14 (December 18, 1991).

EXAMINER

DATE CONSIDERED

**EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



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### U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	4,467,409	08/1984	Potash <i>et al.</i>			
	AB2	4,507,728	03/1985	Sakamoto <i>et al.</i>			
	AC2	4,685,080	08/1987	Rhodes, Jr. <i>et al.</i>			
	AD2	4,724,517	02/1988	May, Michael D.			
	AE2	4,777,594	10/1988	Jones <i>et al.</i>			
	AF2	4,782,441	11/1988	Inagami <i>et al.</i>			
	AG2	4,876,639	10/1989	Mensch Jr., William D.			
	AH2	5,132,898	07/1992	Sakamura <i>et al.</i>			
	AI2	5,241,636	08/1993	Kohn, Leslie D.			
	AJ2	5,355,460	10/1994	Eickemeyer <i>et al.</i>			

### FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AK2	EP 0 239 081 B1	09/1995	Europe			N/A
	AL2	EP 0 324 308 B1	03/1996	Europe			N/A
	AM2	EP 0 368 332 B1	09/1997	Europe			N/A

### OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN2	Cobb, Paul, "TinyRISC: a MIPS-16 embedded CPU core," Presentation for Microprocessor Forum, 13 slides (7 pages) (October 22-23, 1996).
	AO2	Gwennap, Linley, "VLIW: The Wave of the Future?: Processor Design Style Could Be Faster, Cheaper Than RISC," <i>Microprocessor Report</i> , Vol. 8, No. 2, pp. 18-21 (February 14, 1994).
	AP2	Kurosawa, K., <i>et al.</i> , "Instruction Architecture For A High Performance Integrated Prolog Processor IPP," <i>Logic Programming: Proceedings of the Fifth International Conference and Symposium (August 15-19, 1988)</i> , MIT Press, Cambridge, MA, Vol. 2, pp. 1506-1530 (1988).
	AQ2	NEC Data Sheet, MOS Integrated Circuit, uPD30121, VR4121 64-/32-Bit Microprocessor (Copyright NEC Electronics Corporation 2000) (76 pages).
	AR2	NEC User's Manual, VR4100 Series™, 64-/32-Bit Microprocessor Architecture, pp. 1-11 and 54-83 (Chapter 3) (Copyright NEC Corporation 2002).

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**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA3	5,506,974	04/1996	Church <i>et al.</i>			
	AB3	5,574,873	11/1996	Davidian, Gary G.			
	AC3	5,732,234	03/1998	Vassiliadis <i>et al.</i>			
	AD3	5,740,461	04/1998	Jaggar, David Vivian			
	AE3	6,021,265	02/2000	Nevill, Edward Colles			
	AF3	6,266,765 B1	07/2001	Horst, Robert W.			07/07/2000
	AG3	6,272,620 B1	08/2001	Kawasaki <i>et al.</i>			04/04/2000
	AH3	2001/0021970 A1	09/2001	Hotta <i>et al.</i>			05/14/2001
	AI3	2004/0054872 A1	03/2004	Nguyen <i>et al.</i>			09/12/2003
	AJ3						

**FOREIGN PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AK3	EP 0 449 661 B1	11/1995	Europe			N/A
	AL3	GB 2 016 755 A	09/1979	United Kingdom			N/A
	AM3						Yes No

**OTHER (Including Author, Title, Date, Pertinent Pages, etc.)**

	AN3	NEC User's Manual, VR4121™, 64/32-Bit Microprocessor, uPD30121, pp. 1-19 and 103-131 (Chapter 4) (Copyright NEC Corporation 1998).
	AO3	Ross, Roger, "There's no risk in the future for RISC," <i>Computer Design</i> , Vol. 28, No. 22, pp. 73-75 (November 13, 1989).
	AP3	
	AQ3	
	AR3	

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